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PATENT
P54508

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

HAE-SEUNG LEE

Serial No.: 08/931,125 Examiner: PORTKA, GARY

Filed: 16 September 1997 (CPA filed on 27 March 2001) Art Unit: 2187

For: MEMORY SYSTEM FOR IMPROVING DATA INPUT/OUTPUT PERFORMANCE AND METHOD OF CACHING DATA RECOVERY INFORMATION

CERTIFICATE OF MAILING

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is to certify that on this, the 2nd day of September 2003, this Request for Rehearing under 37 C.F.R. §1.197(b) (three copies), is being deposited with the U.S. Postal Service, as first class mail, sufficient postage prepaid, in an envelope addressed to:

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Respectfully submitted,

Robert E. Bushnell
Reg. No.: 27,774
Attorney for the Applicant

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Washington, D.C. 20005
Area Code: 202-408-9040

Folio: P54508
Date: 9/2/3
I.D.: REB/kf

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PATENT
P54508

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS & INTERFERENCES

In re Application of:

HAE-SEUNG LEE

Appeal No. 2003-0573

Serial No.: 08/931,125

Examiner: PORTKA, GARY

Filed: 16 September 1997
(CPA filed on 27 March 2001)

Art Unit: 2187

For: MEMORY SYSTEM FOR IMPROVING DATA INPUT/OUTPUT PERFORMANCE AND METHOD OF CACHING DATA RECOVERY INFORMATION

Attn: Board of Patent Appeals and Interferences

REQUEST FOR REHEARING UNDER 37 C.F.R. § 1.197 (b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response the Decision on Appeal mailed on 2 July 2003 (Paper No. 43), Appellant respectfully requests rehearing pursuant to 37 C.F.R. §1.197(b) for the above-captioned application.

Folio: P54508
Date: 09/02/2003
I.D.: REB/kf

ASSIGNMENT OF ERROR AND ARGUMENT

The ultimate issues discussed in the present application are whether claims 1, 2, and 6 through 8 were properly rejected under 35 U.S.C. § 102 for alleged anticipation by Jones U.S. Patent No. 5,572,660; and whether claims 3 through 6 were properly rejected under 35 U.S.C. § 103 for alleged unpatentability over Jones in view of Holland *et al.* U.S. Patent No. 5,455,934.

In the *Decision on Appeal* mailed on 2 July 2003 (Paper No. 43), the Board reversed the Examiner's rejection of claim 3 through 6 under 35 U.S.C. § 103, but sustained the Examiner's rejection of claims 1, 2 and 6 through 8. Appellant maintains here that consideration of the express language of representative claim 1, as opposed to the Examiner's paraphrase of Appellant's claim 1, will not support the maintenance of the Examiner's rejection of claim 1 under 35 U.S.C. §102(e) as anticipated by Jones U.S. 5,572,660.

A. THE § 102 REJECTION OF CLAIMS 1-2 AND 6 IS ERRONEOUS BECAUSE THE JONES PATENT DOES NOT DISCLOSE ALL ELEMENTS OF THE CLAIMS

All independent claims in this case are limited to RAID-5 systems having one-to-one caching.[1] Claims 1 through 2 and 6 stand rejected under § 102 on the ground that the Jones

[1] Independent claim 1 is directed to "A redundant array of inexpensive disks (RAID) level 5 memory system, comprising: . . . a plurality of caches, each of said plurality of caches respectively coupled operatively to a corresponding single unique one of said plurality of defect-adaptive memory devices, each of said plurality of caches adapted for storing parity information for data recovery for a corresponding single unique one of said plurality of defect-adaptive memory devices to provide one-to-one caching . . . ." Claim 2 depends from claim 1. Claim 6 is an independent apparatus claim but it has substantially the same limitation.

reference teaches one-to-one caching in a RAID-5 system. It is well settled that a § 102 rejection cannot stand if the single reference allegedly supporting the rejection fails to contain each and every element (limitation) of the rejected claim. *In re Robertson*, 169 F.3d 743, 49 USPQ2d 1949 (Fed. Cir. 1999).

Without re-opening the issue of whether Jones '660 fairly teaches one–to-one caching, it suffices to understand that Jones '660 teaches a particular caching scheme in a RAID level 4 context, and then suggests that:

> "[a] fault tolerant disk array subsystem that implements a level 5 RAID technique may also be provided that utilizes a similar write-back caching scheme for storing parity information." Jones '660, col. 3, lines 15-18.

This suggestion may be found implemented in Figure 2D of Jones '660, which uses,

> "[t]he cache units 254-1 through 254-8 ... partitioned and configures such that a write-through caching scheme is carried out when array scheduler 210 writes real data to a selected disk drive and such that a *write-back caching scheme* is carried out when scheduler 210 *writes parity information to a selected disk drive*." Jones '660, col. 10, lines 21-26. Emphasis added. [2]

---

[2] Appellant previously noted this same passage in the *Reply Brief*. In its entirety, that passage of Jones states: "...[T]he parity information is stored and distributed among the plurality of disk drives 214-1 through 214-8 according to a level 5 RAID approach. As such, a plurality of cache units 254-1 through 254-8 are coupled between array scheduler 210 and disk drives 214-1 through 214-8. The cache units 254-1 through 254-8 are partitioned and configured such that a write-through caching scheme is carried out when array scheduler 210 writes real data to a selected disk drive and such that a write-back caching scheme is carried out when array scheduler 210 writes parity information to a selected disk drive."

The Board has already correctly noted that Jones '660:

> "describes the RAID-5 embodiment, illustrated in Figure 2D, as being similar to the RAID-4 system illustrated in Figure 2 *with the exception that parity data is distributed* ***throughout*** *the disk drives* ***in accordance with RAID-5*** *system requirements."* *Decision On Appeal*, Paper No. 43, page 7. Emphasis added.

The Board's finding conforms with the brief statement by Jones '660 that,

> "[t]he embodiment of FIG. 2D is similar to that of FIG. 2 with the exception that the parity information is stored and distributed among the plurality of disk drives 214-1 through 214-8 according to a level 5 RAID approach." Jones '660, col. 10, lines 15-18.

It is this same "parity information"[3] that Jones '660 teaches are read and then used in "a *write-back caching scheme* [which] is carried out when scheduler 210 *writes parity information to a selected disk drive*." Jones '660, col. 10, lines 21-26.

Appellant, in contradistinction to the teachings of Jones '660 about the storage of parity information, defines in representative claim 1, a structure for a RAID level 5 memory system, with a combination of:

> "a plurality of ... memory devices ... having ***a first region*** for sequentially storing parity information ...;"[4]

---

[3] That parity data is the "*parity data*" which the Board found to be taught by Jones '660 to be" *distributed* ***throughout*** *the disk drives* ***in accordance with RAID-5*** *system requirements*." Decision On Appeal, Paper No. 43, page 7.

[4] Claim 1's "first region" may be read as either an ordinal *first*, that is, as a region preceding the "second region for storing data" defined by claim 1, or as a dedicated region for storing parity information, as distinguished from the intermittent parity regions intrinsic in level 5 RAID data striping, as described by Jones '660 and illustrated by Appellant's Figure 2. However Appellant's *first region* is read, either as a sequential order of dedication of the storage capacity, or as a term to the *second region*, claim 1 defines a fixed, or dedicated, region in which parity information is

and

> "a controller ... selectively storing parity information needed for data recovery ***obtained*** from said ***first region*** of a corresponding ... memory devices in a predetermined corresponding ... one of said plurality of caches."

Jones '660 teaches, as the Board so found, a level 5 RAID structure described illustrated by Appellant's Figure 2 and described in Appellant's original specification as having the "[d]ata ... divided by strip (the data is divided by strip 3 in FIG. 2), distributed and stored in each drive DR1 to DR5" so that "each drive DR1 to DR5 has a data block D in which data is stored, and a parity block P in which parity information is stored ... ." Specification, page 9, lines 6-9. Elsewhere (see, for example, page 10, lines 1-9) Appellant recognized the difficulties intrinsic in the art's dedication to level 5 RAID data striping.

Moreover, Appellant taught that the dedicated, or fixed location of "the parity block for storing the parity information" makes it "now possible to prevent time delay due to a separate search when [a] sequential read/write operation is carried out." [5] This improvement can not be read from the level 5 RAID data striping taught by Jones '660.

---

stored, in contracted to the data striping allocation of the locations for storage of parity information practiced by Jones '660 and the prior art described by Appellant's original specification and illustrated by Appellant's Figure 2.

[5] Appellant's original specification, page 12, lines 6-8.

The Examining Staff relied upon a paraphrase of the language of Appellant's claims, rather than made an examination of the subject matter of those claims "as a whole." Accordingly, the Board is respectfully requested to grant Appellant's request for rehearing, and to refuse to sustain this anticipation rejection of representative claim 1.

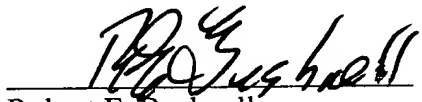
CONCLUSION

The rejection of claim 1 under 35 U.S.C. §102(e), and its maintenance in the *Decison On Appeal*, was erroneous because Jones '660 consistently relies upon a write-back of parity information from a disk location allocated in a level 5 RAID data striping scheme and its intrinsic slowness, while claim 1 defines a different structure with "a controller ... selectively storing parity information ... obtained from said first region" of the memory device. In short, the cited references failed to disclose all elements of the rejected claims, as is required to support an anticipation rejection under 35 U.S.C. §102(e), and as has been repeatedly explained by the Federal Circuit in such exemplars as *In re Schreiber*, 128 F.3d 1473, 44 USPQ2d 1429 (Fed. Cir. 1997); *Gechter v. Davidson*, 116 F.3d 1454, 43 USPQ2d 1030 (Fed. Cir. 1997). If a single element or limitation is missing from the reference, no anticipation occurs. *Motorola, Inc. v. Interdigital Technology Corp.*, 121 F.3d 1461, 43 USPQ2d 1481 (Fed. Cir. 1997); *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 230 USPQ 82 (Fed. Cir. 1986).

The Examining Staff has the burden to show, by a preponderance of evidence, that Lee is not entitled to a patent because the claimed subject matter is anticipated by, or is obvious from, the art of record. Lee is entitled to a patent "unless" the PTO establishes otherwise. See, e.g., *In*

re Dembiczak, 175 F.3d 994, 1001, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999); *In re Epstein*, 32 F.3d 1559, 1564 (Fed. Cir. 1994); *In re Rijckeart*, 9 F.3d 1551, 1552, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

Respectfully submitted,



Robert E. Bushnell,
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Registration No.: 27,774

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Orginal & Fax

BD of APPEAL

#45 Req. rehearing

PATENT
P54508

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS & INTERFERENCES

In re Application of:

HAE-SEUNG LEE

Appeal No. 2003-0573

Serial No.: 08/931,125

Examiner: PORTKA, GARY

Filed: 16 September 1997
(CPA filed on 27 March 2001)

Art Unit: 2187

For: MEMORY SYSTEM FOR IMPROVING DATA INPUT/OUTPUT PERFORMANCE AND METHOD OF CACHING DATA RECOVERY INFORMATION

Attn: Clerk of the Board of Patent Appeals and Interferences

LETTER

Via Facsimile: 703-308-7952

Commissioner for Patents
Attn.: Mr. Craig Feinberg
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Mr. Feinberg:

Enclosed are three copies of a Substitute Request for Rehearing Under 37 C.F.R. §1.197(b).

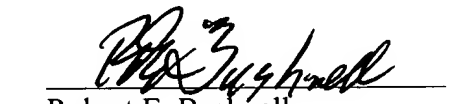
The originals were filed under Certificate of Mailing on Tuesday, the 2nd of September 2003, pursuant to 37 C.F.R. §1.8(a). The Substitute Request is made necessary to correct malapropisms and typographic errors found in the original. These errors include:

- pluralization of the word claim in the second paragraph on page 2;
- changing the tense of the word configures in the second quote on page 3;
- changing the font of footnote 2 on page 3;

- bolding and italicizing three words in third quote on page 4;
- repositioning quotation mark in footnote 3;
- inserting additional text in footnote 4;
- deletion of unnecessary word "described" in first paragraph on page 5;
- insertion of footnote in second paragraph on page 5; and
- substitution of contrast for contracted and insertion of additional text in footnote 4.

Thank you for entering the Substitute Request.

Respectfully submitted,



Robert E. Bushnell,
Attorney for the Applicant
Registration No.: 27,774

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Folio: P54508
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I.D.: REB/kf/wc

PATENT
P54508

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS & INTERFERENCES

In re Application of:

HAE-SEUNG LEE

Appeal No. 2003-0573

Serial No.: 08/931,125

Examiner: PORTKA, GARY

Filed: 16 September 1997
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For: MEMORY SYSTEM FOR IMPROVING DATA INPUT/OUTPUT PERFORMANCE AND METHOD OF CACHING DATA RECOVERY INFORMATION

Attn: Board of Patent Appeals and Interferences

SUBSTITUTE REQUEST FOR REHEARING UNDER 37 C.F.R. § 1.197(b)

Commissioner for Patents
Attn.: Mr. Craig Feinberg
P.O. Box 1450
Alexandria, VA 22313-1450

Via Facsimile: 703-308-7952

Sir:

In substitution for Appellant's Request For Rehearing Under 37 CFR §1.197(b) which was timely filed under a Certificate of Mailing on the 2nd of September 2003, pursuant to 37 CFR §1.8(a), in response to the Decision on Appeal mailed on 2 July 2003 (Paper No. 43), Appellant respectfully requests rehearing pursuant to 37 C.F.R. §1.197(b) for the above-captioned application. This substitution is made to correct typographic errors in Appellant's original Request.

Folio: P54508
Date: 9/4/03
I.D.: REB/kf/wc

ASSIGNMENT OF ERROR AND ARGUMENT

The ultimate issues discussed in the present application are whether claims 1, 2, and 6 through 8 were properly rejected under 35 U.S.C. § 102 for alleged anticipation by Jones U.S. Patent No. 5,572,660; and whether claims 3 through 6 were properly rejected under 35 U.S.C. § 103 for alleged unpatentability over Jones in view of Holland *et al.* U.S. Patent No. 5,455,934.

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reference teaches one-to-one caching in a RAID-5 system. It is well settled that a § 102 rejection cannot stand if the single reference allegedly supporting the rejection fails to contain each and every element (limitation) of the rejected claim. *In re Robertson*, 169 F.3d 743, 49 USPQ2d 1949 (Fed. Cir. 1999).

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The Board has already correctly noted that Jones '660:

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[2] Appellant previously noted this same passage in the *Reply Brief*. In its entirety, that passage of Jones states: "...[T]he parity information is stored and distributed among the plurality of disk drives 214-1 through 214-8 according to a level 5 RAID approach. As such, a plurality of cache units 254-1 through 254-8 are coupled between array scheduler 210 and disk drives 214-1 through 214-8. The cache units 254-1 through 254-8 are partitioned and configured such that a write-through caching scheme is carried out when array scheduler 210 writes real data to a selected disk drive and such that a write-back caching scheme is carried out when array scheduler 210 writes parity information to a selected disk drive."

> "describes the RAID-5 embodiment, illustrated in Figure 2D, as being similar to the RAID-4 system illustrated in Figure 2 *with the exception that parity data is distributed* ***throughout*** *the disk drives* ***in accordance with RAID-5*** *system requirements." Decision On Appeal*, Paper No. 43, page 7. Emphasis added.

The Board's finding conforms with the brief statement by Jones '660 that,

> "[t]he embodiment of FIG. 2D is similar to that of FIG. 2 with the exception that the parity information is stored and distributed among the plurality of disk drives 214-1 through 214-8 according to a level 5 RAID approach." Jones '660, col. 10, lines 15-18.

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Appellant, in contradistinction to the teachings of Jones '660 about the storage of parity information, defines in representative claim 1, a structure for a RAID level 5 memory system, with a combination of:

> "a plurality of ... memory devices ... having ***a first region*** for ***sequentially storing parity*** information ...;"[4]

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[3] That parity data is the "*parity data*" which the Board found to be taught by Jones '660 to be "*distributed* ***throughout*** *the disk drives* ***in accordance with RAID-5*** *system requirements.*" Decision On Appeal, Paper No. 43, page 7.

[4] Claim 1's "first region" may be read as either an ordinal *first*, that is, as a region preceding the "second region for storing data" defined by claim 1, or as a dedicated region for storing parity information, as distinguished from the intermittent "distributed" (see Jones '660, col. 10, lines 15 , 16) parity regions (i.e., dispersed parity regions) intrinsic in level 5 RAID data striping, as described by Jones '660 and illustrated by Appellant's Figure 2. However Appellant's *first region* is read, either as a sequential order of dedication of the storage capacity, or as a term relative to the *second region*, claim 1 defines a fixed, or dedicated, region in which parity information is stored, in contrast to the data striping allocation of the locations for storage of parity information

and

> "a controller ... selectively storing parity information needed for data recovery ***obtained*** from said ***first region*** of a corresponding ... memory devices in a predetermined corresponding ... one of said plurality of caches."

Jones '660 teaches, as the Board so found, a level 5 RAID structure illustrated by Appellant's Figure 2 and described in Appellant's original specification as having the "[d]ata ... divided by strip (the data is divided by strip 3 in FIG. 2), distributed and stored in each drive DR1 to DR5" so that "each drive DR1 to DR5 has a data block D in which data is stored, and a parity block P in which parity information is stored ... ." Specification, page 9, lines 6-9. Elsewhere (see, for example, page 10, lines 1-9) Appellant recognized the difficulties intrinsic in the art's dedication to level 5 RAID data striping.

Moreover, Appellant taught that the dedicated, or fixed location of "the parity block for storing the parity information"[5] makes it "now possible to prevent time delay due to a separate search when [a] sequential read/write operation is carried out." [6] This improvement can not be read from the level 5 RAID data striping taught by Jones '660.

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practiced by Jones '660 and the prior art described by Appellant's original specification and illustrated by Appellant's Figure 2. Jones '660 neither teaches nor suggests Appellant's "sequentially storing parity information."

5 "a first region for sequentially storing parity information... ." Claim 1, line 4.

6 Appellant's original specification, page 12, lines 6-8.

The Examining Staff relied upon a paraphrase of the language of Appellant's claims, rather than made an examination of the subject matter of those claims "as a whole." Accordingly, the Board is respectfully requested to grant Appellant's request for rehearing, and to refuse to sustain this anticipation rejection of representative claim 1.

CONCLUSION

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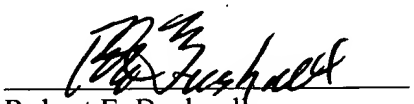
The Examining Staff has the burden to show, by a preponderance of evidence, that Lee is not entitled to a patent because the claimed subject matter is anticipated by, or is obvious from, the art of record. Lee is entitled to a patent "unless" the PTO establishes otherwise. See, e.g., *In*

re Dembiczak, 175 F.3d 994, 1001, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999); *In re Epstein*, 32 F.3d 1559, 1564 (Fed. Cir. 1994); *In re Rijckeart*, 9 F.3d 1551, 1552, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

Respectfully submitted,



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